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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/014,359	12/14/2001	Michael Joachim Wolf	Q67426	1154

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EXAMINER
JONES, PRENELL P

ART UNIT	PAPER NUMBER
2619	

MAIL DATE	DELIVERY MODE
11/13/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/014,359	WOLF ET AL.	
	Examiner	Art Unit	
	Prenell P. Jones	2619	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 August 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *2,10,14,18 and 21-23* is/are allowed.

6)☒ Claim(s) *1,13,15-17,19,20 and 24-31* is/are rejected.

7)☒ Claim(s) *3-9,11 and 12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Response to Arguments

1. Applicant's arguments with respect to claims 1-31 have been considered but are moot in view of the new ground(s) of rejection.

Applicant argues that the cited art fail to teach or suggest "adjusting means for the phase adjustment of the second delay means, so that the delayed second clock signal is adapted to the phase of the delayed first clock signal at an output end of a first delay means." In light of Applicant argument, Examiner has reviewed the previously cited prior art of Hamamoto et al (US Pat 5,987,619), whereby Examiner has withdrawn previous 102 rejections. However, Examiner has performed an additional search.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 13, 27 and 28 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Regarding independent claim 13, Applicant is claiming, "A computer-readable medium," which is not discussed in the specification. Claims 27 and 28 depend on claim 13, and therefore are rejected as well.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 1, 13, 15-17, 19, 20, and 24-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hamamoto et al (US Pat 5,987,619) in view of Hillis et al (US 5,118,975).

Regarding claims 1, 13, 15-17, 19, 20 and 24-31, Hamamoto discloses a phase compensation circuit that includes a first and second delay circuit along with associated internal clocks (INTCLK, INTDCLK, DCLK1 and DCLK2), wherein signals are eventually outputted and a clock signal generation circuit that receives clock signals, and delay circuits that receive internal first/second clock signals, delay first internal clock and delay second internal clock, additional signals along with various clock signals are monitored, such as data signals, wherein clock signals are shifted to be in phase with data signals, (Abstract, Fig. 7-9, col. 2, line 21-54, col. 5,

line 7 thru col. 6, line 47, col. 7, line 15-45), and adjusting/shifting (Fig. 7, col. 5, line 45 thru col. 6, line 7) one delayed internal clock to match another delayed internal clock, resulting in the matching internal clock signals, and a first and second clock signals are external clock signals (Fig. 7, 8, 9, 10 & 11).

Although Hamamoto fail to disclose "adjusting means for the phase adjustment of the second delay means, so that the delayed second clock signal is adapted to the phase of the delayed first clock signal at an output end of a first delay means," in a clock environment, Hillis discloses a controllable delay associated with clock circuits, wherein the architecture includes multiple delay circuits for enabling adjustment of delay, and wherein internal data signals are phase shifted 180 degrees and monitored to adjust the phase of internal clock signal INTCLK (col. 5, line 58-63), and phase comparators are further monitoring status/position of clock signals, such as weather signals are Leading, Lagging, in-phase or out-phase (col. 4, line 28-39). In addition, an in-phase signal represents the SYS CLK IN (second clock phase adjusted) clock signal occurs simultaneously with corresponding DEL CLK OUT delayed (first clock delayed) clock out reference signal, in which the signals are in-phase (col. 4, line 50-64).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to be motivated to implement adjusting means for the phase adjustment of the second delay means, so that the delayed second clock signal is adapted to the phase of the delayed first clock signal at an output end of a first delay means as taught by Hillis with the teachings of Hamaoto for the purpose of further providing reliable data communication with managing timing associated with communication signaling.

Allowable Subject Matter

1. Claims 2, 10, 14, 18 and 21-23 are allowed over prior art.

2. Claims 3-9, 11 and 12, are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: Although the combined cited art discloses phase compensation associated in a telecommunication environment wherein utilization of a first/second delay unit along with corresponding first/second clock signals and associated delay time, and adjusting the phase, they fail to teach or suggest with respect to claims 3 and 4, first delay time corresponds to a maximum expected phase difference and/or maximum expected propagation time difference between at least one first clock signal and the second clock signal, with respect to claim 5, selecting one of the at least one first delayed clock signal and the second delayed clock signal and optionally one of the at least first clock signal and the second clock signal, where the respective selected, at least one first delayed clock signal or second delayed clock signal serves to synchronize the compensation module, with respect to claim 8, when first delayed clock signal is selected instead of the second delayed clock signal, the delayed first clock signal present at an output end of the first delay means is adapted by adjusting, with respect to claim 9, the first or second start value is performed only upon attainment of a predetermined first deviation tolerance value, while the converse applies upon the attainment of a second deviation tolerance value which is smaller than the first deviation tolerance value, with respect to claims 10 and 11, phase adjustment changes the second delay time of second delay means in dynamic step sizes, a respective step size being modified as a function of the respective phase difference, with respect to claim 14, a SDH transmission network that includes a compensation module for clock signals in the network with SDH, with respect to claim 18, code executed by control means on a console of a network device for a transmission with a SDH.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Prenell P. Jones whose telephone number is 571-272-3180. The examiner can normally be reached on 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor Wing Chan can be reached on 571-272-7493. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Prenell P. Jones

November 3, 2007

11/7/07

WING CHAN
SUPERVISORY PATENT EXAMINER